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PERFORMANCE ANALYSIS OF NoC ROUTING ALGORITHMS FOR 5 × 5 MESH BASED SoC

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Abstract

Over the years, semiconductor industry has undergone a rapid evolution which urges the SoCs to become communication-centric. For efficient on-chip communication, high performance routers are used. System on chip is an adaptable building design for the outline of center based Framework on-chip. A routing algorithm plays a dominant role in network's operation. Several routing algorithms have been designed to cater several features and purposes. There are still a lot of requirements that has to be met. Such performance metrics are minimum latency, least power and maximum throughput. This paper deals with XY routing, PROM routing and DyAD routing. Performance is evaluated in terms of varying packet sizes and routing algorithms. The simulation results revealed a tradeoff between XY and PROM routing. In the measure of throughput and power, XY routing and DyAD routing scores on the top respectively. In case of non-uniform traffic loads, DyAD routing is well suited. This comparative study has been performed with the aid of NIRGAM NoC simulator in a 5 × 5 mesh based topology. Under wormhole switching, it is preferable to adopt DyAD routing in wireless routers in terms of low power and high throughput. This paper also forecast the need of adaptive implementation which must be application specific in the future years.

Keywords:

NoC, Nirgam, Routing, Algorithm, SoC

1. INTRODUCTION

A billion transistors with several outlines on a solitary IC chip is a challenging task in NoC to IC planners. The best IC designers overcome all difficulties to give efficient and low-power IC's, which is functional and dependable operation of the SoC's.

As the combination builds the expense adequacy is likewise a real range of concern in IC designs. The SoC is an innovation where the greatest innovation is packing it into the more little conceivable space. The outline framework of an on-chip is affected emphatically by the supposed protected innovation (Intellectual Property) center. A coordinated circuit center is a predesigned and verified silicon circuit block. The core usually contain more than 6,000 gates that can be used in building a bigger or complicated application on a semiconductor chip.

Nanometer technology permits integration of various transistors on a single chip. Due to increased integration, it exacerbates the look productivity gap and temporal order closure issues. A system on chip is a computer circuit that integrates all elements of a computer or other digital system into one chip. The crucial challenge which is faced by the designers of these systems should overcome is to produce functionally correct and reliable operations of the interacting elements. On chip physical interconnections can gift a limiting issue for performance and energy consumption.

The rest of this paper is organized as follows. In section 2, we discuss the design strategies in NoC designs. Section 3 describes the Routing Algorithms for Noc Architectures. Section 4 consists of architecture of NoC. The results and graphs are discussed in section 5 and concluded in Section 6 presents the concluding remarks.

2. BACKGROUND STUDY

Recent systems-on-chips (SoCs) designs are integrated by IP (Intellectual Property) cores which is useful in designing reconfigurable architectures.

2.1 EVOLUTION OF ON CHIP NETWORKS

The need of packet switched on-chip systems is explored. Here the discussion begins from varied communication infrastructure for a System on Chip and the details about how the NoC turned out to be so popular in this area. Here there is an information about processors and its connection to the NoC. This discussion will go ahead with fundamental parts and vital outline design ideas of NoC [1], [2]. There are three basic communication systems frameworks for system on chip (SoC). They are point to point communication, shared bus and wired/wireless on chip network architectures.

2.1.1 Point to Point Communication:

In point to point communication [6], the resources or cores are allowed to share the data directly through wires that are connected to each core. In this method, sharing the data does not want any priority providing system or arbitration unit. For performing read/write operation in a system on chip having additional range of cores, this communication system needs huge routing area, massive routing delay and large range of pins for every core. While performing read/write operation in this communication system, we will find the quality of signal and delays occurred for routing. Thus testing of that system may be a most mind-numbing job. Due to the above problems, direct point to point interconnection system shows some disadvantages like underutilization of cores, poor reusability, high quality and poor scalability [2]. A System on Chip that has less range of cores or resources, will use this communication infrastructure and may offer best performance as compared to alternative systems.

2.1.2 Shared Bus:

In the Shared Bus, the cores are connected to one or more buses. Arbiter is used for splitting and sending the data between the cores [13]. Here, the Shared bus communication infra-structure needs less input/output pins as compared to point to point communication system. Thus wiring space and price is greatly reduced. But, due to arbitration, the data transfer speed will be reduced [7].

2.1.3 Network on Chip:

Network on Chip is a well suited architecture for the design of core based System-on-Chip. NoC is a set of interconnected switches, with IP cores connected to switches. NoCs possess better performance, bandwidth, and scalability than shared bus [8]. Switches are meant to receive, store, route and sent packets. To accomplish these functions, a switch is composed of router, buffer, arbiter and flow control unit.

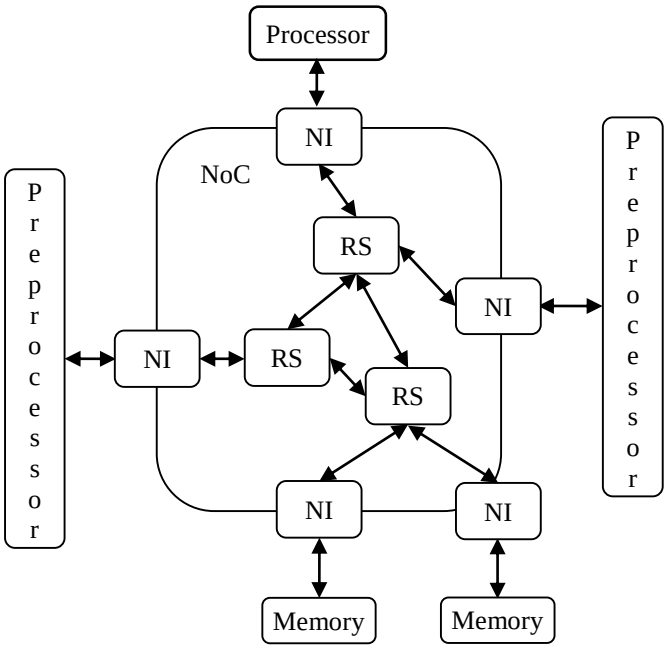

Fig.1. Basic Components of NoC Router

The most important features that distinguish NoC architectures are network topology and routing algorithms. The performance of the NoC depends on the routing algorithm. All the algorithms are application specific. Choosing the right type of routing is essential. It directly affects the network performance and power consumption [13-16]. In terms of power and latency, routing algorithms are compared here. To evaluate the performance gains that can be achieved with the three routing algorithms, the networks are simulated using NIRGAM emulator. The simulation results explored the effectiveness of each of the three algorithms under different traffic patterns. There are many factors that have a significant impact on the NoC performance.

2.1.4 Basic Concepts of NoC:

The important design concepts of NoC such as i) Topology, ii) Switching techniques, iii) Routing algorithms are described below. The performance of NoC mainly depends routing algorithms and switching techniques [14], [15].

2.1.4.1 Mesh Topology:

Mesh Topology consists of P number of rows and Q number of columns. In Mesh topology, IP cores are connected to their respective router and the routers are connected with interconnection of wires. The address of the router and IP cores are well-known by (*x*, *y*) co-ordinates of the network. In Mesh Topology, The main advantage is the easy detection and isolation of faults in the defined network which is easy to implement [19]. In this topology the messages are more protected as the messages go through a dedicated line and the messages will only reach its intended addresses.

2.1.4.2 Switching Techniques:

In this section, the types of flow control mechanism are discussed. The internal connection between the input and output channels in the router are described by the switching techniques. In circuit switching technique, the electrical inter-connection is required to communicate between the source and destination routers. Packet switching is developed in order to overcome the inefficiencies in circuit switching such as resource allocation delay in multiple network hops. Here, the data splits into small, separate packets which will improve link utilization. In store-and-forward switching technique, each and every resources or nodes need to wait till whole data packet has been received by the destination node. Afterwards, the other packets are forwarded to the next node [15]. Due to this, the shift technique will lead to long delay at every hop, which is not suitable for NoC and the Store and forward flow control entails sufficient buffering at each router to buffer the entire packet. In virtual cut through Switching Technique, the buffer delay is reduced where the transmission of a packet is allowed to ensue to the next node before the entire data packet is received by the destination router. But, it requires large buffer to transfer the data which adapt more area and power. In wormhole switching technique [13], the packets are split into flits, allowing flits to move on to the neighboring router before the entire packet is received at the destination as in virtual cut-through switching technique. In wormhole switching the flit can move forward to the current node if there is sufficient space in the buffer for the flit [21]. This technique has low storage space of a flit size, a link has to be reserved for the duration of lifetime of packet in the router. Due to these advantages such as area and power of the Noc, wormhole switching technique is the most preferable technique for the Network on Chip router.

3. ROUTING ALGORITHMS FOR NOC

3.1 ROUTING ALGORITHM

The routing algorithm is one of the key ingredient in NoC architecture [20]. The routing algorithm defines the path adopted by the packet between source and destination. Routing algorithms can also be defined based on their implementation: lookup table and Finite State Machine (FSM). A perfect algorithm must prevent deadlock, livelock and starvation situations. Deadlock is the repeated dependency on the nodes which seek access to the resources set which leads to blockage in the progress even in the presence of events happening. Livelock is the process of packet circulation in the network without reaching the destination. Starvation occurs when a packet in buffer request for output channel and without getting allocated.

The properties of routing algorithms that are concerned for interconnection networks are connectivity, adaptivity, deadlock and live lock freedom, and fault tolerance [4]. Connectivity is the ability to route packets from any source node to any destination node. Adaptivity is the ability to route packets through alternative paths in the presence of contention or faulty components. Deadlock freedom is the ability to guarantee that packets will not block or wander across the network forever. Fault tolerance is the ability to route packets in the presence of faulty components.

There is myriad of ways to classify algorithms. It is possible to classify as source and distributive based on where routing decisions are taken. Based on how the path is defined, it is classified as deterministic or adaptive. Based on the path length, routing algorithm can be termed as minimal or non-minimal routing algorithm. Based on the flexibility, it is classified as static or dynamic routing. According to number of destinations routing algorithms are classified into two types i.e. unicast and multicast routing.

XY routing is a kind of distributed deterministic routing algorithm which never ends into deadlock or livelock. Most commercially available parallel machines usually adopt distributed deterministic routing because of its simplicity and speed but it assumes the traffic is uniform. Path-based, Randomized, Oblivious, Minimal routing (PROM) is a family of oblivious, minimal, path-diverse routing algorithms especially suitable for Network-on-Chip applications with n × n mesh geometry [19]. DyAD is a new paradigm for NoC router design which fuses the advantages of both deterministic and adaptive routing schemes. DyAD judiciously switches between deterministic and adaptive routing based on network congestion conditions. During congestion, the router adopts to adaptive routing mode and during non-congestion state, it switches to deterministic mode.

The performance parameters taken into consideration are throughput, latency and power consumption. Throughput is defined as a fraction of packets delivered from sources to destinations in a given amount of time. Latency is defined as time taken to deliver a packet from source to destination. It is desirable to exhibit high throughput and low latency. This can be achieved using appropriate routing algorithms. Power consumption is also one of the important NoC design parameter especially targeted in case of battery operated devices. Three different routing algorithms are described in detail below.

3.1.1 XY Algorithm:

The XY routing algorithm is one type of distributed deterministic routing algorithm which never gives deadlock or livelock [8]. For a 2-D mesh based NoC, each router can be identified by its coordinate (*x*, *y*) (Fig.2). The XY routing algorithm check the current router address (*Xx*, *Xy*) to the destination router address (*Yx*, *Yy*) of the packet, stored in the header flit [9]. Flits will be routed to the core port of the router when the (*Xx*, *Xy*) address of the current router is equal to the (*Yx*, *Yy*) address.

In XY routing algorithm, for each and every node, if the destination router (*Dx*) is greater than the current router (*Cx*), the message will be directed to East node and if smaller (*Dx* < *Cx*), it will be directed to West node. If both are same, it will be in the same column as source. Likewise, if the destination router (*Dy*) is greater than the current router (*Cy*), the message will directed to North node and if smaller (*Dy* < *Cy*), it will be directed to South node. If both are same, it will be in the same column as current router.

3.1.2 PROM Algorithm:

The PROM algorithm [9] uses only 2 virtual channels for deadlock-free routing which depends on the relative position of the source node *S* and destination node *D*, and is the same for all flows traveling from source to destination: 1. if *D* lies to the east of *S*, vertical links use the first VC; 2. if *D* lies to the west of *S*, vertical links use the second VC; 3. if *D* lies directly North or South of *S*, both VCs are used; 4. all horizontal links may use all VCs.

3.1.3 DyAD Algorithm:

DyAD merges the advantages of both deterministic and adaptive routing schemes [11]. DyAD is a routing technique, which sensibly switches based on network congestion's conditions between deterministic and adaptive routing. The freedom from deadlock and livelock [17] can be guaranteed when mixing deterministic and adaptive routing modes into the same NoC. The main advantage of using deterministic routing is its minimalism of the structure of router design. Because of the simplified logic, the deterministic routing provides low latency when the network is not congested.

4. ARCHITECTURE OF 5 × 5 MESH BASED NOC

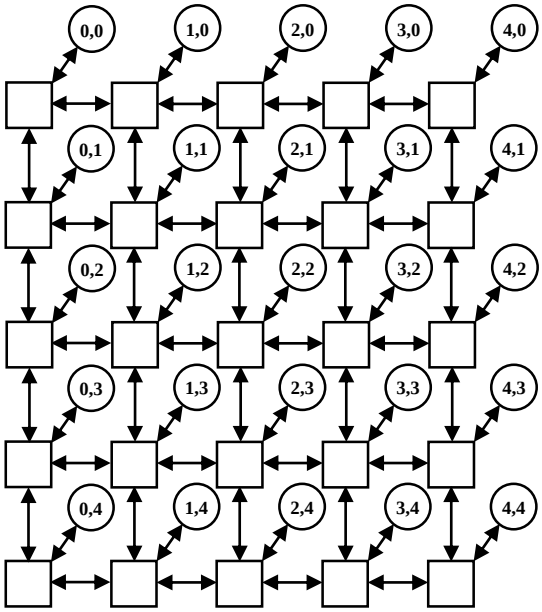

Fig.2. Architecture of 5 × 5 Mesh based Noc

These routing algorithms are simulated based on a 5 × 5 Mesh network as shown in Fig.2. Here, the each circle represents a tile, which consist of the IP cores connected to a router in the network. Each tile is connected with 4 bi-directional channels in all directions to neighbor tiles such as N, E, W and S. Each tiles are identified using individual id's with *x* and *y* co-ordinates. Here, we are using the model of Orion router Core which consists of the code for implementing the topology and routing algorithms.

5. EXPERIMENTAL ANALYSIS

5.1 PLATFORM DESCRIPTION

NIRGAM is a discrete event, cycle accurate simulator targeted at Network on Chip (NoC) research. NIRGAM Simulator works in LINUX operating system [16]. It provides substantial support to experiment with NoC design in terms of routing algorithms and applications on various topologies. NIRGAM is an extensible and modular system C based simulator. It allows to experiment with

various options available at every stage of NoC design viz. topology, switching technique, virtual channels, buffer parameters, routing mechanism and applications. The simulator can output performance metrics (latency and throughput) for a given set of choices. ORION 2.0 was developed by Bin Li at Princeton University and Kambiz Samadi at the University of California [16]. XY, PROM and DyAD algorithms are simulated in NIRGAM. A set of parameters viz., packet size, generated traffic and traffic load were fixed for the simulations.

The platform under consideration composed of 5 × 5 array of tiles is interconnected by a 2D mesh network. Each tile consists of a processing element (PE) and a router. Each router is linked to the four neighboring tiles and its local PE through channels. The switching technique adopted for the on-chip routers is Wormhole Switching. A Crossbar switch is used as the switching fabric. In this paper, XY, PROM and DyAD routing algorithms are considered and the results are analyzed. It is assumed that the packets are consumed immediately, once they reach their destination nodes. Each simulation is run for a warm-up period of 100 cycles. Thereafter, performance data is collected after 48 packets are sent.

5.2 SIMLUATION RESULTS

For simulation, 50% load variation is assumed with the maximum bandwidth with 50,000 complete clock cycles under the clock frequency of 1GHz with the warm up period of 800 clock cycles.

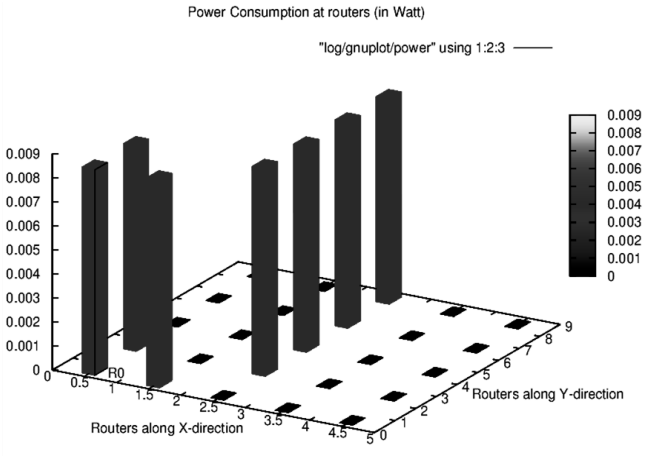

Fig.3. Power Consumption graph for XY routing

Plotted in the Fig.3 is the power consumption graph under S and N channels in 5 × 5 mesh based NoC topology. The Fig.3 shows the power consumption graph for XY routing algorithm in the Orion router core in NIRGAM simulator. The Fig.4 shows the power consumption graph for PROM routing algorithm in the 5 × 5 mesh based Orion router core in NIRGAM simulator.

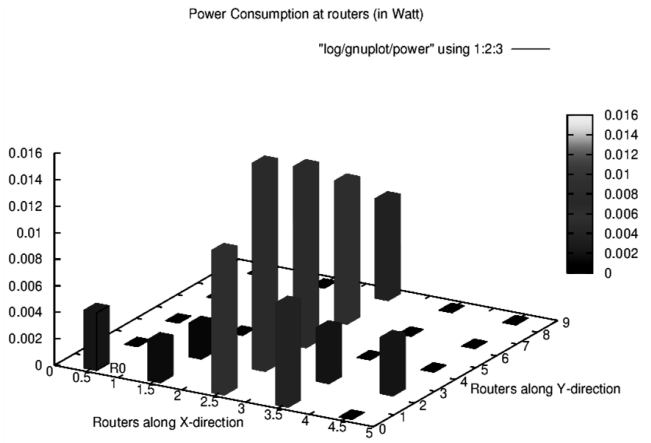

Fig.4. Power Consumption graph for PROM routing

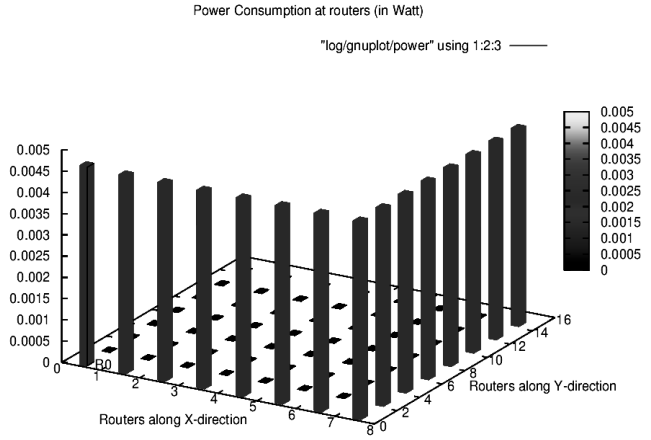

Fig.5. Power Consumption graph for DyAD routing

The Fig.5. shows the power consumption graph for DyAD routing algorithm in Nirgam simulator. Here, the throughput and speed are very high with low power consumption.

The minimum value of typical latency per channel is attained as 1.62371, overall average latency per channel (in clock cycles per packet) is obtained as 8.95432, with the total network power of 0.1623mW in DyAD routing algorithm. The results reveal that the DyAD routing algorithm out performs PROM and XY routing algorithms.

Table.1. Comparison of XY, PROM and DyAD Routing Algorithm for 5 × 5 network topology

Routing Algorithm	**Latency / Flit (ms)**	**Latency / Packet (ms)**	**Throughput (Gbps)**	**Power Consumption (mW)**
XY	2.07631	13.12980	15.120	7.96231
PROM	1.98234	12.64113	13.7330	7.83212
DyAD	1.62312	9.54621	11.540	0.82313

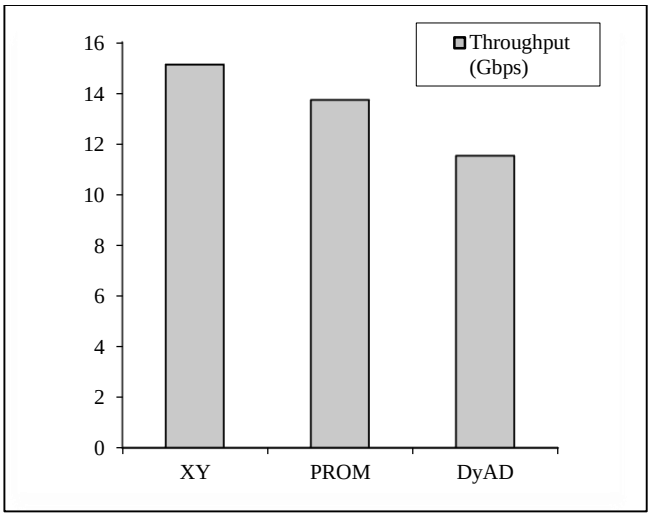

Fig.6. Throughput Analysis graph for routing techniques

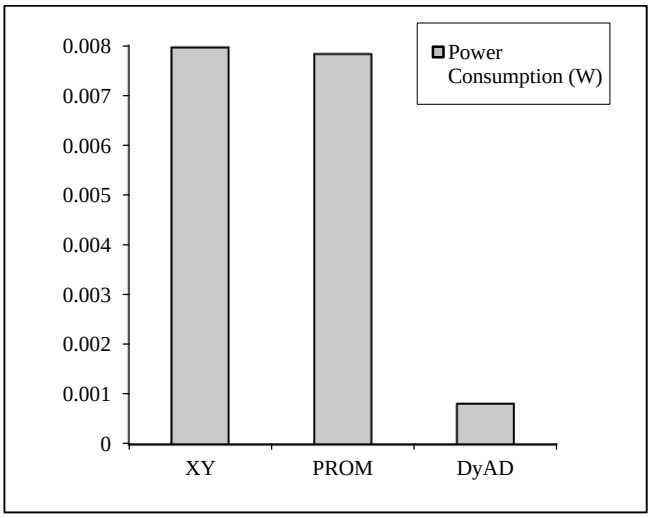

Fig.7. Power Consumption Analysis graph for routing techniques

The comparison results in Table.1 show that in context to Latency/flit and Latency/packet DyAD proves to be best compared to XY and PROM. Whereas, in case of Throughput XY proves to be the best by 15.120 as compared to DyAD routing Algorithm. But in terms of power consumption, DyAD proves to be best by 0.82mW. The Fig.6 shows the Throughput analysis graph for XY, PROM and DyAD routing algorithms and Fig.7 shows the Power Analysis graph for these routing techniques.

6. CONCLUSION

The three versions of routing algorithms (XY, PROM, DyAD) are compared using 5 × 5 mesh based technology with a clock rate of 100Mhz. Performance evaluation and comparison is done by means of varying packet sizes and routing algorithms.

A tradeoff between XY and PROM routing is observed from the simulation results. PROM achieved higher saturation throughput than XY routing but XY excels in terms of average packet latency at low network workloads. XY routing shows an outstanding performance at uniform traffic load but fails with non-uniform traffic load due to its determinisms. The simulation results show that DyAD routing algorithm consistently outperforms the other two routing schemes. With the obtained results, it is possible to customize the algorithm well suited for a particular application. XY algorithm suffers from channel underutilization while adaptive algorithms distribute the traffic more uniformly across the network. Concerning the relative performance of the algorithms in terms of network conditions, the DyAD routing consumes low power in 5 × 5 mesh based topology under wormhole switching. Hence it is concluded that the DyAD routing algorithm is very well suited for wireless routers.

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